



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Christopher H. Pham  
Assignee: Cisco Technology, Inc.  
Title: Linear Associative Memory-Based Hardware Architecture For Fault Tolerant ASIC/FPGA Workaround  
Serial No.: 09/837,882 Filing Date: April 18, 2001  
Confirmation No.: 8340 Date Allowed: November 25, 2005  
Examiner: Mai T. Tran Group Art Unit: 2129  
Docket No.: CIS0115US

Austin, Texas  
November 30, 2005

Attention: Official Draftsperson  
Mail Stop Issue Fee  
COMMISSIONER FOR PATENTS  
P. O. Box 1450  
Alexandria, VA 22313-1450

**SUBMISSION OF FORMAL DRAWINGS**

Dear Sir:

Applicants submit four (4) sheets of formal drawings, consisting of Figures 1 and 2, 3, 4, and 5 in the above-named application. If there are any questions regarding these drawings, please call the undersigned at (512) 439-5080.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to Attention: Official Draftsperson, Commissioner For Patents, P. O. Box 1450, Alexandria, VA 22313-1450, on November 30, 2005.

  
Attorney for Applicant(s)

11/30/05  
Date of Signature

Respectfully submitted,



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